REMARKS

This amendment is filed in response to the Office Action dated November 14, 2005. In view of this amendment, this application should be allowed and the case passed to issue.

No new matter is introduced by this amendment. New claims 8-15 are supported throughout the specification and accompanying figures, including Figures 1 and 2.

Claims 8-15 are pending in this application. Claims 1-7 are rejected. Claims 1-7 have been canceled in this response.

Notice of References Cited

It is noted that Young et al., U.S. Patent No. 4,851,257 has not been cited on a PTO-892, although the Examiner has applied it in a rejection. **It is again requested that the Examiner cite Young et al. on a PTO-892 in the next official action.**

Claim Rejections Under 35 U.S.C. §§ 102 and 103

Claims 1 and 7 were rejected under 35 U.S.C. § 102(b) as being anticipated by Young et al. (U.S. Patent No. 4,851,257).

Claims 1 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Young et al.

These rejections are traversed, and reconsideration and withdrawal thereof respectfully requested. The following is a comparison between the present invention, as claimed, and the cited prior art.

Claims 1-7 have been canceled, therefore the following remarks are presented in support of the patentability of new claims 8-15.

An aspect of the invention, per claim 8, is a semiconductor device comprising a semiconductor substrate having two types of active regions that are a PMOS and an NMOS

region separated from each other in plan view by a PN separation film. A first gate electrode of P-type polycrystal silicon extends across the PMOS region and extends over the PN separation film. A second gate electrode of N-type polycrstal silcon extends across the NMOS region and extends over the PN separation film. A silicide film is formed over the PN separation film and has a first side contacting the first gate electrode and a second side contacting the second gate electrode. An interlayer insulating film is formed over the first gate electrode, the first insulating film, and the first source and drain regions, and the interlayer insulating film has a contact hole overlapping one of the second source and drain regions and the second gate electrode in plan view. The first and second sides of the silicide film are within the PN separation film in plan view and the first and second sides of the silicide film do not extend to the two types of active regions. The interlayer insulating film covers a whole surface of the silicide film.

An aspect of the invention, per claim 12, is a semiconductor device comprising a semiconductor substrate having two types of active regions that are a PMOS and an NMOS region separated from each other in plan view by a PN separation film. A first gate electrode of P-type polycrystal silicon extends across the PMOS region and extends over the PN separation film. A second gate electrode of N-type polycrstal silcon extends across the NMOS region and extends over the PN separation film. A silicide film is formed over the PN separation film and has a first side contacting the first gate electrode and a second side contacting the second gate electrode. An interlayer insulating film is formed over the first gate electrode, the first insulating film, and the first source and drain regions, and the interlayer insulating film has a contact hole overlapping one of the second source and drain regions and the second sidewall insulating film in plan view. The first and second sides of the silicide film are within the PN separation film in

plan view and the first and second sides of the silicide film do not extend to the two types of active regions. The interlayer insulating film covers a whole surface of the silicide film.

Claims 8 and 12 are similar to each other, except that claim 8 requires that the contact hole overlaps the second gate electrode, while claim 12 requires that the contact hole overlaps the second sidewall insulating film.

The new claims clarify four features of the present invention:

1) The claimed semiconductor device is a dual-gate type CMOS, and the contacts to the source/drain regions are formed in a self-aligned manner with respect to the gate electrode. In plan view, the contacts overlap with the gate electrode.

2) The P-type gate electrode in the PMOS region and the N-type gate electrode in the NMOS region, which form the dual-gate type CMOS, are connected by a silicide film.

3) The both ends of the silicide film that connects the P-type gate electrode and the N-type gate electrode are placed within the area of the PN separation film in plan view, and do not overlap with the active regions.

4) There is no contact hole in a portion that connects the P-type gate electrode and the N-type gate electrode (the silicide film).

Young et al. disclose (Fig. 1e) a technique of connecting a drain region of a PMOS transistor and a drain region of a NMOS transistor, with a stacked structure made of a polycrystalline silicon region 40 and a conducting member 75 formed of a silicide. Young et al. describe (column 6, lines 1-3) that the polycrystalline layer corresponds to the regions denoted by 80a, 90a, and formed on an underlying oxide region. Hence, it appears that the conducting member 75 extends over the entire area of the underlying oxide region 20.

Figs. 1d, 1e, 2b, 2c, 4c, and 4d of Young et al. show a portion that connects electrodes extracted from the drain region of the PMOS transistor and the drain region of the NMOS transistor, and do not show a portion that connects the P-type gate electrode and the N-type gate electrode. Accordingly, however far the conducting member 75 extends in Fig. 1e, Young et al. do not disclose that both ends of the silicide film that connects the P-type and N-type gate electrodes are placed within the area of the PN separation film in plan view, and do not overlap with the active regions, as required by claims 8 and 12 (see feature (3) above).

Young et al. further do not describe where to arrange the contact hole, and hence do not disclose that there is no contact hole in the silicide film connecting the P-type and N-type gate electrodes (see feature (4) above).

Claims 1-3 were rejected under 35 U.S.C. § 102(b) as being anticipated by Liaw (U.S. Patent No. 6,214,656).

Claims 1-6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Liaw in view of Goto (U.S. Patent No. 5,902,121).

Claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Liaw in view of Goto and Young et al.

These rejections are traversed, and reconsideration and withdrawal thereof respectfully requested.

The Examiner averred that Liaw teaches a semiconductor device comprising a semiconductor substrate 10 having PMOS and NMOS regions separated by a PN separation film 12, a dual gate 30/32 extending linearly across the PMOS region, the PN separation film, and the NMOS region, and silicide region 62. The Examiner asserted that Liaw does not recite the reasons for a small area of silicide. The Examiner relied on Goto's teaching to conclude that one

of ordinary skill in this art would have been motivated to reduce the distance between and active region.

Liaw does not disclose that both ends of the silicide film that connects the P-type and N-type gate electrodes are placed within the area of the PN separation film in plan view, and that the silicide does not overlap with the active regions, as required by claims 8 and 12 (see feature (3) above). Rather, Liaw discloses (Fig. 15) that an end of a silicide layer 62 and an end of an active region overlap.

Liaw further do not describe where to arrange the contact hole, and hence do not disclose that there is no contact hole in the silicide film connecting the P-type and N-type gate electrodes (see feature (4) above).

Goto and Young et al. do not cure the deficiencies of Liaw, as Goto and Young et al. do not suggest that both ends of the silicide film that connects the P-type and N-type gate electrodes are placed within the area of the PN separation film in plan view, and do not overlap with the active regions and also do not suggest no contact hole in the silicide film connecting the P-type and N-type gate electrode

The factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention, such that the identically claimed invention is placed into the recognized possession of one having ordinary skill in the art. *Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 66 USPQ2d 1801 (Fed. Cir. 2003); *Crown Operations International Ltd. v. Solutia Inc.*, 289 F.3d 1367, 62 USPQ2d 1917 (Fed. Cir. 2002). There are significant differences between the claimed semiconductor device and the device disclosed by Young et al. and Liaw that would preclude the factual determination that Young et al. and Liaw identically describe the claimed invention

within the meaning of 35 U.S.C. § 102. Because Young et al. and Liaw do not disclose a semiconductor device comprising a silicide film formed over the PN separation film and having a first side contacting the first gate electrode and a second side contacting the second gate electrode, wherein the first and second sides of the silicide film are within the PN separation film in plan view and the first and second sides of the silicide film do not extend to the two types of active regions, and wherein the interlayer insulating film covers a whole surface of the silicide film, as required by claims 8 and 12, Young et al. and Liaw do not anticipate claims 8 and 12.

The Examiner's contention that Applicant admitted that a dual gate electrode is "notoriously conventional" is vigorously traversed. Applicant has made no such admission. Applicant has not admitted that the claimed dual gate electrode is admitted prior art. While dual gate electrodes may be known, Applicant has not admitted that dual gate electrodes with the claimed structure are prior art.

Applicant further submits that Young et al. and Liaw do not suggest the claimed semiconductor device.

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge readily available to one of ordinary skill in the art. *In re Kotzab*, 217 F.3d 1365, 1370 55 USPQ2d 1313, 1317 (Fed. Cir. 2000); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). There is no suggestion in Young et al., Liaw, and Goto, to provide a semiconductor device comprising a silicide film formed over the PN separation film and having a first side contacting the first gate electrode and a second side contacting the second gate electrode, wherein the first and second

sides of the silicide film are within the PN separation film in plan view and the first and second sides of the silicide film do not extend to the two types of active regions, and wherein the interlayer insulating film covers a whole surface of the silicide film, as required by claims 8 and 12.

The only teaching of the claimed semiconductor device required by claims 8 and 12 is found in Applicant's disclosure. However, the teaching or suggestion to make a claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

The dependent claims are allowable for at least the same reasons as the respective independent claims from which they depend and further distinguish the claimed

In view of the above amendments and remarks, Applicant submits that this application should be allowed and the case passed to issue. If there are any questions regarding this Amendment or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. §1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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